forming a second insulating film thicker than the gate on said exposed top and side surfaces and on an entire surface of the substrate;

planarizing the second insulating film, to again expose the top surface of the gate;

depositing a refractory metal layer on an entire surface such that the refractory metal layer is adjacent to the patterned conductive film;

forming a silicide layer on an upper surface of the gate by heat treatment; and

etching the refractory metal layer and the second insulating film.

10. (Amended) A method of fabricating a gate in a semiconductor device, comprising:

forming a non-silicide conductive film on a semiconductor substrate;

patterning the conductive film, to form a gate, wherein the top and side surfaces of said gate are exposed;

forming an insulating film thicker than the gate on said exposed top and side surfaces and on an entire surface of the substrate;

planarizing the second insulating film, to again expose the top surface of the gate; and

forming a silicide pattern on the conductive pattern, the silicide pattern having a predetermined width, and being formed after the conductive pattern is

formed, said step of forming a silicide pattern comprising:

forming a refractory metal on the conductive pattern such that the refractory metal is adjacent to the conductive pattern; and

heat treating the refractory metal to form the silicide pattern having the predetermined width at an intersection between the refractory metal and the conductive pattern.

21. (Amended) A method of fabricating a gate electrode of a predetermined width, comprising:

forming a gate insulating layer and a non-silicide gate on a semiconductor substrate; and

forming a first silicide pattern on the non-silicide gate without etching a silicide from which the silicide pattern is fabricated.